IN THE CLAIMS:

The current claims follow. For claims not marked as amended in this response, any difference in the claims below and the previous state of the claims is unintentional and in the nature of a typographical error.

1. (Currently Amended) A device arranged to compose basic-code vectors into a composite-code vector, the device comprising:

a vector processor, wherein the vector processor comprises:

at least two weighted sum units, each weighted sum unit being arranged to provide an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors;

an add unit, the add unit being arranged to sum the intermediate-code vectors into the composite-code vector; and

the weighted sum units being under the control of a first and a second configuration word,[[and]]

wherein the first and the second configuration word are deployed to configure the operations performed by the weighted sum units.

2. (Previously Presented) A device according to claim 1, wherein a pre-processing unit is coupled to at least one of the weighted sum units and to the add unit, the pre-processing unit being arranged to perform additional operations on the intermediate-code vector, and the pre-processing unit being under the control of a third and a fourth configuration word, wherein the third and the fourth configuration word are deployed to configure the additional operations on the intermediate-code vector.

3. (Previously Presented) A device according to claim 1, wherein a post-processing unit is coupled to the add unit, the post-processing unit being arranged to perform additional operations on the composite-code vector, and the post-processing unit being under the control of a fifth configuration word, wherein the fifth configuration word is deployed to configure the additional operations on the composite-code vector.

4. (Previously Presented) A device according to claim 1, wherein the weighted sum units are arranged to calculate a bit-wise addition of at least two basic-code vectors.

5. (Previously Presented) A device according to claim 2, wherein the pre-processing unit is arranged to erase, repeat and reorder the elements of the intermediate-code vector.

6. (Previously Presented) A device according to claim 2, wherein the pre-processing unit is arranged to apply a mask on the intermediate-code vector.

7. (Previously Presented) A device according to claim 3, wherein the post-processing unit is arranged to perform a conditional negation of the composite-code vector.

8. (Previously Presented) A device according to claim 1, wherein the weighted sum units and the add unit are arranged to be configured during a configuration stage of the operation of the device.

9. (Previously Presented) A device according to claim 2, wherein the pre-processing unit is arranged to be configured during a configuration stage of the operation of the device.

10. (Previously Presented) A device according to claim 3, wherein the post-processing unit is arranged to be configured during a configuration stage of the operation of the device.

11. (Previously Presented) A method for composing basic-code vectors into a composite-code vector, the method comprising the steps of:

(a) providing, by a vector processor, a first and a second intermediate-code vector, each of which is a weighted sum of a plurality of the basic-code vectors;

(b) summing, by the vector processor, the intermediate-code vectors into a composite-code vector;

(c) receiving, by the vector processor, a first and a second configuration word; and

(d) controlling, by the vector processor, step (a) with the first and the second configuration word.